ES_LPC435x/3x/2x/1x Flash

Errata sheet LPC435x/3x/2x/1x flash-based devices

Rev. 6.4 — 10 December 2015 **Errata sheet**

Document information

Info	Content
Keywords	LPC4357FET256; LPC4357JET256; LPC4357JBD208; LPC4353FET256; LPC4353JET256; LPC4353JBD208; LPC4337FET256; LPC4337JET256; LPC4337JBD144; LPC4337JET100; LPC4333FET256; LPC4333JET256; LPC4333JBD144; LPC4333JET100; LPC4327JBD144; LPC4327JET100; LPC4325JBD144; LPC4325JET100; LPC4323JBD144; LPC4323JET100; LPC4322JBD144; LPC4322JET100; LPC4317JBD144; LPC4317JET100; LPC4315JBD144; LPC4315JET100; LPC4313JBD144; LPC4313JET100; LPC4312JBD144; LPC4312JET100; ARM Cortex-M4 flash-based devices errata
Abstract	This errata sheet describes both the known functional problems and any deviations from the electrical specifications known at the release date of this document. Each deviation is assigned a number and its history is tracked in a table.

Revision history

Rev	Date	Description
6.4	20151210	• Added PMC.2.
6.3	20151023	• Added RESET.3.
6.2	20150904	• Added the word linear to the ramp-up time for the first work-around in OTP.1. For all packages, except BGA256, if the VDDREG, VDDIO, and VDDA pins are tied together, the supply voltage must have a linear ramp-up time of at least 2 ms. See Section 3.19.
6.1	20150827	• Added OTP.1. • Removed PWR.1. Increased I/O current in the BGA 256 package for M4 was assembly related and did not go into production.
6	20150417	• Added USB.2. • Added SD/MMC.1. • Added EMC.2. • Added RESET.1. • Added RESET.2.
5	20140815	• Added Rev A. • Added USBROM.1, USBROM.2, EEPROM.2. • Removed IRC.1. IRC specification changed in data sheet. • Removed EEPROM.1.
4	20130722	• Added USB.1, ISP.1, EMC.1.
3.1	20130416	• Added SRAM.1.
3	20130125	• Added I2C.1.
2.1	20121123	• Added clarification that this errata applies to flash-based devices only. • Filename changed from ES_LPC435X_3X_2X_1X to ES_LPC435X_3X_2X_1X_FLASH.
2	20121020	• Added PWR.1, IRC.1. • Removed AES.1, ETM.1, RGU.1, SPIFI.1; documented in user manual. • Updated EEPROM.1, C_CAN.1, IBAT.1. • Added LPC432x and LPC431x devices. • Document title changed from ES_LPC4357_53_37_33 to ES_LPC435X_3X_2X_1X.
1.1	20120808	• Added RGU.1 and EEPROM.1. • Corrected C_CAN0/C_CAN1 peripheral assignment.
1	20120717	• Initial version.

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1. Product identification

The LPC435x/3x/2x/1x flash-based devices (hereafter referred to as 'LPC43xx') typically have the following top-side marking:

LPC43xxxxxxxx

xxxxxxxx

xxxYYWWxR[x]

The last/second to last letter in the last line (field 'R') will identify the device revision. This Errata Sheet covers the following revisions of the LPC43xx flash-based devices:

Table 1. Device revision table

Revision identifier (R)	Revision description
'A'	Second device revision
'-'	Initial device revision

Field 'YY' states the year the device was manufactured. Field 'WW' states the week the device was manufactured during that year.

2. Errata overview

Table 2. Functional problems table

Functional problems	Short description	Revision identifier	Detailed description
C_CAN.1	Writes to CAN registers write through to other peripherals.	'-'	Section 3.1
EEPROM.2	Reset values for the RWSTATE and WSTATE registers in the EEPROM block are different from what is shown in the user manual.	'-', 'A'	Section 3.2
EMC.1	External Memory Controller clock frequency divide by 2 mode limit.	'-'	Section 3.3
EMC.2	Operating frequency of EMC lower than data sheet value.	'-', 'A'	Section 3.4
I2C.1	In the slave-transmitter mode, the device set in the monitor mode must write a dummy value of 0xFF into the DAT register.	'-', 'A'	Section 3.5
ISP.1	'J' command in ISP mode swaps last two items.	'-' (with a boot ROM version of 11.2)	Section 3.6
MCPWM.1	MCPWM abort pin not functional.	'-'	Section 3.7
PMC.1	PMC.x power management controller fails to wake up from deep sleep, power down, or deep power down.	'-'	Section 3.8
PMC.2	Wake-up from deep-sleep mode using USB0/1 peripherals.	'-'	Section 3.9
SRAM.1	SRAM in deep sleep and power down modes may lose state.	'-', 'A'	Section 3.10
USB.1	USB0 unable to communicate with low-speed USB peripheral in host mode when using full-speed hub.	'-', 'A'	Section 3.11

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Table 2. Functional problems table *…continued*

Functional problems	Short description	Revision identifier	Detailed description
USB.2	The USB_SOF_Event may fire earlier than expected and/or a false interrupt may be generated.	'-', 'A'	Section 3.12
USBROM.1	Nested NAK handling of EP0 OUT endpoint.	'-', 'A'	Section 3.13
USBROM.2	Isochronous transfers.	'-', 'A'	Section 3.14
SD/MMC.1	Data CRC error returned on CMD6 command.	'-', 'A'	Section 3.15
RESET.1	Master Reset (MASTER_RST) and M4 Reset (M4_RST) are not functional.	'-', 'A'	Section 3.16
RESET.2	PERIPH_RST is not functional.	'-', 'A'	Section 3.17
RESET.3	Loss of device functionality on reset via nRESET in deep-sleep and power-down mode.	'-', 'A'	Section 3.18
OTP.1	Repeated power cycling of the device may cause erroneous programming of the OTP banks.	'-'	Section 3.19

Table 3. AC/DC deviations table

AC/DC deviations	Short description	Product version(s)	Detailed description
IBAT.1	VBAT supply current higher than expected.	'-'	Section 4.1

Table 4. Errata notes table

Errata notes	Short description	Revision identifier	Detailed description
n/a	n/a	n/a	n/a

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3. Functional problems detail

3.1 C_CAN.1

Introduction:

Controller Area Network (CAN) is the definition of a high performance communication protocol for serial data communication. The C_CAN controller is designed to provide a full implementation of the CAN protocol according to the CAN Specification Version 2.0B. The C_CAN controller allows to build powerful local networks with low-cost multiplex wiring by supporting distributed real-time control with a very high level of security.

Problem:

On the LPC43xx flash-based devices, there is an issue with the C_CAN controller AHB bus address decoding that applies to both C_CAN controllers. It affects the C_CAN controllers when peripherals on the same bus are used. Writes to the ADC, DAC, I2C, and I2S peripherals can update registers in the C_CAN controller. Specifically, writes to I2C0, MCPWM, and I2S can affect C_CAN1. Writes to I2C1, DAC, ADC0, and ADC1 can affect C_CAN0. The spurious C_CAN controller writes will occur at the address offset written to the other peripherals on the same bus. For example, a write to ADC0 CR register which is at offset 0 in the ADC, will result in the same value being written to the C_CAN0 CNTL register which is at offset 0 in the C_CAN controller. Writes to the C_CAN controller will not affect other peripherals.

Work-around:

Work-arounds include: Using a different C_CAN peripheral. Peripherals I2C1, DAC, ADC0, and ADC1 can be used at the same time as C_CAN1 is active without any interference. The I2C0, MCPWM, and I2S peripherals can be used at the same time as C_CAN0 is active without any interference. Another workaround is to gate the register clock to the CAN peripheral in the CCU. This will prevent any writes to other peripherals from taking effect in the CAN peripheral. However, gating the CAN clock will prevent the CAN peripheral from operating and transmitting or receiving messages. This workaround is most useful if your application is modal and can switch between different modes such as an I2S mode and a CAN mode. Another workaround is to avoid writes to the peripherals while CAN is active. For example, the ADC could be configured to sample continuously or when triggered by a timer, before the CAN is configured. Afterwards, C_CAN0 can be used since the ADC will operate without requiring additional writes.

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3.2 EEPROM.2

Introduction:

A 16 kB EEPROM is available on these parts which operates up to 204 MHz. Registers in the EEPROM define the number of wait states that are applied to read and write operations on the device.

Problem:

The reset values for the RWSTATE and WSTATE registers in the EEPROM block are different from what is shown in the user manual.

Table 5. Reset values for RWSTATE and WSTATE

	Reset value for Rev '-' parts	Reset value for Rev 'A' parts
RWSTATE	0000 0905	0000 0E07
WSTATE	0002 0602	0004 0802

Work-around:

No work-around needed. Program the required values into the registers before using the EEPROM.

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3.3 EMC.1

Introduction:

The LPC43xx parts contain an External Memory Controller (EMC) capable of interfacing to external SDRAM, SRAM, and asynchronous parallel flash memories. The EMC can be configured to operate at the processor core frequency (BASE_M4_CLOCK) or the core frequency divided by 2.

Problem:

When operated in the divide by 2 mode (EMC_CLK_SEL, bit 16 CREG6, Address 0x4004.312C), the duty cycle of the clock is not the typical 50 % which shortens the setup time. This could impact designs with an EMC running faster than 100 MHz in divide by 2 mode (which corresponds to a maximum core frequency of 200 MHz).

Work-around:

If the external bus is running greater than 100 MHz in divide by 2 clock mode, consider the following:

1. When using only one external chip, use the CLK1 or CLK3 pin to drive the SDRAM clock for best performance. CLK0 and CLK2 pins are used for SDRAM read capture feedback clocks and must not be used for any other function.
2. When using two x16 SDRAMs, use the CLK1 pin to drive the clock on SDRAM D15:D0, and CLK3 pin to drive the SDRAM D31:D16. CLK0 and CLK2 pins are used for SDRAM read capture feedback clocks and must not be used for any other function.

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3.4 EMC.2

Introduction:

The LPC43xx parts contain an External Memory Controller (EMC) capable of interfacing to external SDRAM, SRAM, and asynchronous parallel flash memories. The EMC can be configured to operate at the processor core frequency (BASE_M4_CLOCK) or the core frequency divided by 2.

Problem:

For SDRAM, the electrical characteristic of the LQFP144 and LQFP208 packages limits the operating frequency of the EMC to a certain level, which is lower than the specified value in the data sheet. Choosing an SDRAM clock of 72MHz as the upper limit provides some safety margin. This frequency is either achieved by a core and EMC frequency of 72MHz, or by a 144MHz core and a 72MHz EMC frequency. However, SDRAM performance can vary depending on board design and layout.

Work-around:

There is no work-around.
The upper limit of the SDRAM clock frequency is highly dependent on the PCB layout and the quality of the power supply and de-coupling circuitry.

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3.5 I2C.1

Introduction:

The I2C monitor allows the device to monitor the I2C traffic on the I2C bus in a non-intrusive way.

Problem:

In the slave-transmitter mode, the device set in the monitor mode must write a dummy value of 0xFF into the DAT register. If this is not done, the received data from the slave device will be corrupted. To allow the monitor mode to have sufficient time to process the data on the I2C bus, the device may need to have the ability to stretch the I2C clock. Under this condition, the I2C monitor mode is not 100% non-intrusive.

Work-around:

When setting the device in monitor mode, enable the ENA_SCL bit in the MMCTRL register to allow clock stretching.

Software code example to enable the ENA_SCL bit:

```
LPC_I2C_MMCTRL |= (1<<1); //Enable ENA_SCL bit
```

In the I2C ISR routine, for the status code related to the slave-transmitter mode, write the value of 0xFF into the DAT register to prevent data corruption. In order to avoid stretching the SCL clock, the data byte can be saved in a buffer and processed in the Main loop. This ensures the SI flag is cleared as fast as possible.

Software code example for the slave-transmitter mode:

```
case 0xA8:     // Own SLA + R has been received, ACK returned
case 0xB0:
case 0xB8:     // data byte in DAT transmitted, ACK received
case 0xC0:     // (last) data byte transmitted, NACK received
case 0xC8:     // last data byte in DAT transmitted, ACK received
    DataByte = LPC_I2C->DATA_BUFFER;//Save data. Data can be process in Main loop
    LPC_I2C->DAT = 0xFF;            // Pretend to shift out 0xFF
    LPC_I2C->CONCLR = 0x08;         // clear flag SI
break;
```


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3.6 ISP.1

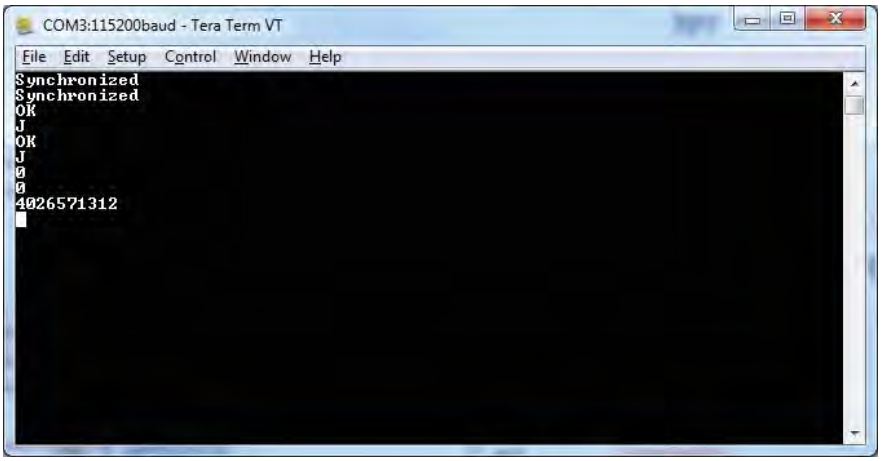
Introduction:

All LPC43xx parts include a feature called In-System Programming (ISP) which boots up over the UART port and provides a terminal-based communication mechanism to query certain characteristics of the part. One of these is the ability to retrieve the Part Identification number.

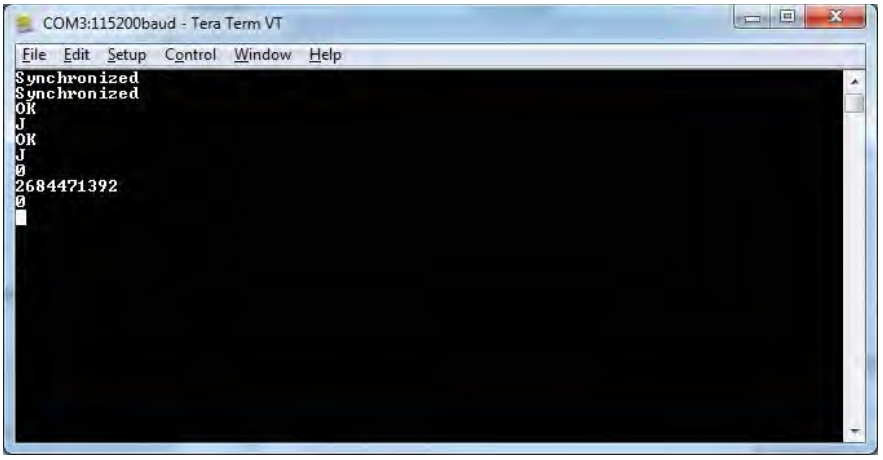
Problem:

The 'J' command in ISP mode should return an error code, followed by an ASCII string representation of the part ID, followed by a 0. However what is actually returned is the error code, followed by a 0, followed by an ASCII string representation of the part ID. The problem is the last two items returned are swapped.

Incorrect example:



Correct example:



Work-around:

There is no work-around for this problem.

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3.7 MCPWM.1

Introduction:

The Motor Control PWM engine is optimized for three-phase AC and DC motor control applications, but can be used in many other applications that need timing, counting, capture, and comparison. The MCPWM contains a global Abort input that can force all of the channels into a passive state and cause an interrupt.

Problem:

The MCPWM Abort input is not functional.

Work-around:

The MCPWM Abort function can be emulated in software with the use of a non-maskable interrupt combined with an interrupt handler that shuts down the PWM. This will result in a small delay on the order of 50 main clock cycles or about 1/3 of a microsecond at 150 MHz. Alternatively, the State Configurable Timer (SCT) can be configured to implement MCPWM functionality including an Abort input. The SCT can respond to external inputs in one clock cycle.

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3.8 PMC.1

Introduction:

The PMC implements the control sequences to enable transitions between different power modes and controls the power state of each peripheral. In addition, wake-up from any of the power-down modes based on hardware events is supported.

Problem:

When the chip is in a transition from active to Deep Sleep, Power Down, or Deep Power Down, wake-up events are not captured and they will block further wake-up events from propagating. The time window for this transition is 6 uS and is not affected by the chip clock speed. After a wake-up event is received during the PMC transition, the chip can only recover by using an external hardware reset or by cycling power.

Work-around:

Make sure that a wake-up signal is not received during the Deep Sleep, Power Down, or Deep Power Down transition period. An example circuit to work around this could include an external 6 uS one shot which could be triggered via software using a GPIO line when entering Deep Sleep, Power Down, or Deep Power Down mode. The one-shot's output could be used to gate the wake-up signal(s) to prevent receiving a wake-up signal during the PMC transition period. Depending on the system design, it may also be needed to latch the wake-up signal(s) so that they will still be present after the one-shot's 6 uS time-out.

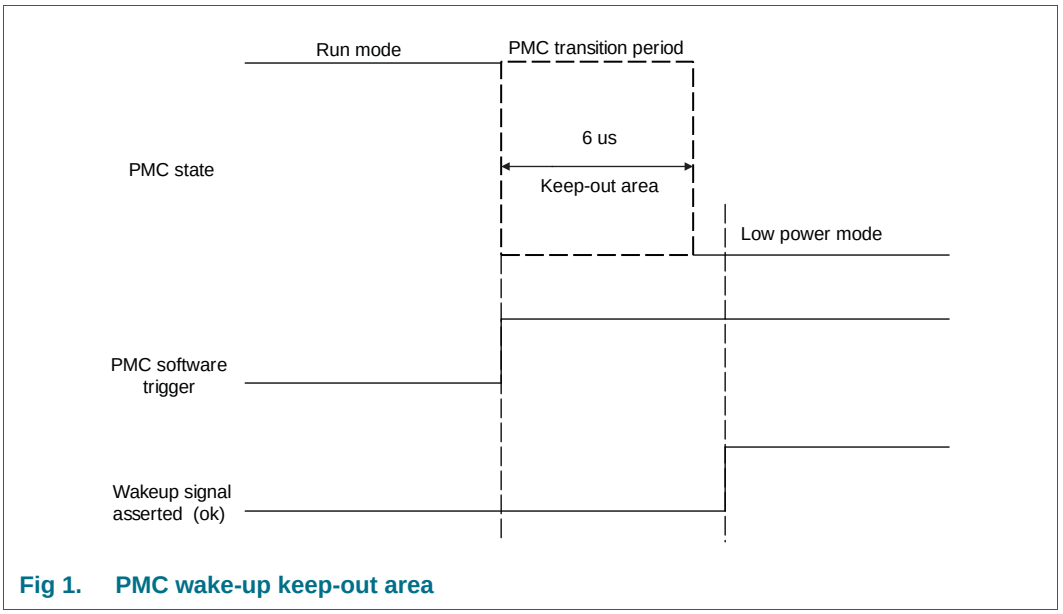

Fig 1. PMC wake-up keep-out area

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3.9 PMC.2

Introduction:

On the LPC43xx devices, USB0 and USB1 peripherals can act as wake-up sources in Sleep mode and in Deep-sleep mode (by setting bits 9 and 10 in CREG1 register).

Problem:

The LPC43xx Rev '-' devices do not support wake-up from Deep-sleep mode using USB0 and USB1. The USB0 and USB1 peripherals can wake-up these devices only from Sleep mode.

Work-around:

There is no work-around.

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3.10 SRAM.1

Introduction:

SRAM state is retained in deep sleep and power down modes.

Problem:

Incorrect settings may lead to SRAM state retention loss over time and temperature. This can cause erratic behavior due to SRAM data loss after wake-up from deep sleep mode or power down mode.

Work-around:

Reserved register at 0x40043008 bits 17:16 should be set to 0x2 before entering deep sleep mode or power down mode.

```
#define CREG0_008       (0x40043008)
#define PD0_SLEEP0_MODE (0x4004201c)

#define PMC_PWR_DEEP_SLEEP_MODE 0x3F00AA
#define PMC_PWR_POWER_DOWN_MODE 0x3FFCBA

unsigned int regval;

// EXAMPLE 1:
regval = *((unsigned int *) CREG0_008);
regval |= (1 << 17);
regval &= ~(1 << 16);
*((unsigned int *) CREG0_008) = regval;

// prepare for entering deep sleep
*((unsigned int *) PD0_SLEEP0_MODE)  = PMC_PWR_DEEP_SLEEP_MODE;

// enter deep sleep
__wfi();

// EXAMPLE 2:
regval = *((unsigned int *) CREG0_008);
regval |= (1 << 17);
regval &= ~(1 << 16);
*((unsigned int *) CREG0_008) = regval;

// prepare for entering power down
*((unsigned int *) PD0_SLEEP0_MODE)  = PMC_PWR_POWER_DOWN_MODE;

// enter power down
__wfi();
```


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3.11 USB.1

Introduction:

The LPC43xx parts include two USB 2.0 controllers that can operate in host mode at high-speed. One of these controllers, USB0, contains an on-chip high-speed UTMI+ compliant transceiver (PHY) which supports high-speed, full-speed, and low-speed USB-compliant peripherals.

Problem:

The USB controller called USB0 is unable to communicate with a low-speed USB peripheral in host mode when there is a full-speed hub directly connected to the USB0 port and a low-speed peripheral is connected in the tree somewhere below this full-speed hub. Only USB0 has this problem; the other USB controller, USB1 does not.

Work-around:

There is no work-around for this problem. It is suggested that the low-speed USB peripheral is either connected directly to USB0 or a high-speed hub is placed between that peripheral and USB0.

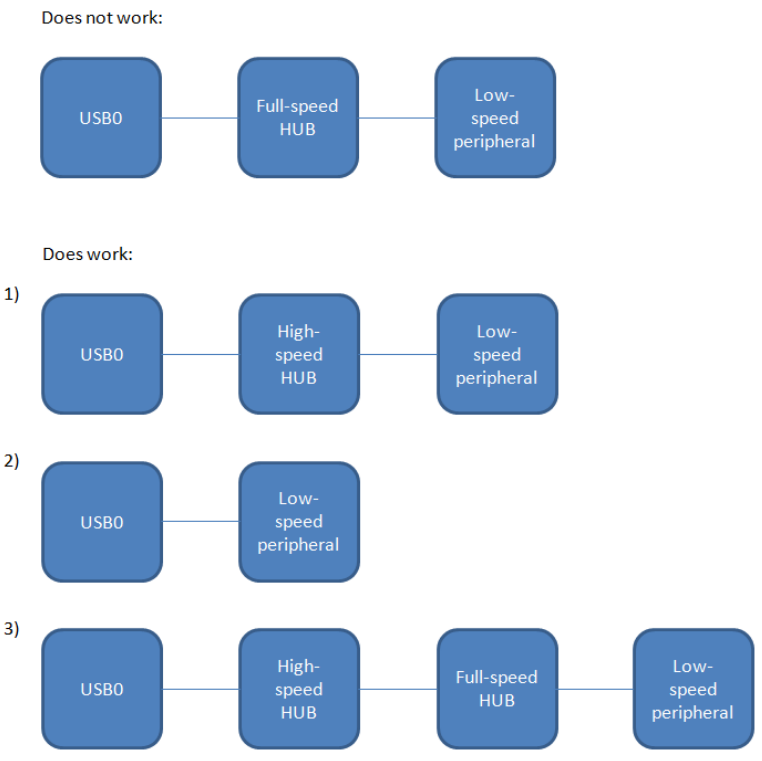

Fig 2. Suggested USB0 to low-speed peripheral connections

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3.12 USB.2

Introduction:

The LPC435x flash-based devices contain an event handler for USB SOF detection from the host called the USB_SOF_Event. When it is enabled this event fires at the start of each USB frame, once per millisecond in full-speed mode or once per 125 microseconds in high-speed mode, and is synchronized to the USB bus.

Problem:

The USB_SOF_Event may fire earlier than expected and/or an additional (false) interrupt may be generated.

Work-around:

There is no work-around. The USB_SOF_Event cannot be used in full-speed and high-speed device mode in case the system needs an interrupt that is aligned with the incoming SOF tokens.

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3.13 USBROM.1

Introduction:

The USB ROM drivers include a default endpoint 0 handler which acts on events generated by the USB controller as a result of traffic occurring over the control endpoint. The user has the option of overloading this default handler for the purpose of performing user specific processing of control endpoint traffic as required.

One of the actions the default endpoint 0 handler performs is to prepare the DMA engine for data transfer after the controller has sent out a NAK packet to the host controller. This is done in preparation for the arrival of the next OUT request received from the host.

Problem:

Due to a race condition there is the chance that a second NAK event will occur before the default endpoint0 handler has completed its preparation of the DMA engine for the first NAK event. This can cause certain fields in the DMA descriptors to be in an invalid state when the USB controller reads them, thereby causing a hang.

Work-around:

Override the default endpoint 0 handler to add checks for and prevents nested NAK event processing activity.

This is an example of how to do this:

```
// Endpoint 0 patch that prevents nested NAK event processing
static uint32_t g_ep0RxBusy = 0; /* flag indicating whether EP0 OUT/RX buffer is
busy. */
static USB_EP_HANDLER_T g_Ep0BaseHdlr; /* variable to store the pointer to base EP0
handler */

/*-------------------------------------------------------------------------
  EP0_patch :
 *-------------------------------------------------------------------------*/
ErrorCode_t EP0_patch(USBD_HANDLE_T hUsb, void* data, uint32_t event)
{

    switch (event) {
        case USB_EVT_OUT_NAK:
            if (g_ep0RxBusy) {
                /* we already queued the buffer so ignore this NAK event. */
                return LPC_OK;
            } else {
                /* Mark EP0_RX buffer as busy and allow base handler to queue the
     buffer. */
                g_ep0RxBusy = 1;
            }
            break;
        case USB_EVT_SETUP: /* reset the flag when new setup sequence starts */
        case USB_EVT_OUT:
            /* we received the packet so clear the flag. */
            g_ep0RxBusy = 0;
```


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```
            break;
    }
    return g_Ep0BaseHdlr(hUsb, data, event);
}


// Install the endpoint 0 patch immediately after USB initialization via the
     hw->Init() call.

*-------------------------------------------------------------------------
  usbd_init: usb subsystem init routine
*-------------------------------------------------------------------------*/
ErrorCode_t usbd_init (void)
{
    USBD_API_INIT_PARAM_T usb_param;
    USB_CORE_DESCS_T desc;
    ErrorCode_t ret = LPC_OK;
    USB_CORE_CTRL_T* pCtrl;


…
    /* USB Initialization */
    ret = USBD_API->hw->Init(&g_AdcCtrl.hUsb, &desc, &usb_param);
    if (ret == LPC_OK) {

        /* register EP0 patch */
        pCtrl= (USB_CORE_CTRL_T*)g_AdcCtrl.hUsb; /* convert the handle to control
      structure */
        g_Ep0BaseHdlr = pCtrl->ep_event_hdlr[0]; /* retrieve the default EP0_OUT
      handler */
        pCtrl->ep_event_hdlr[0] = EP0_patch;     /* set our patch routine as EP0_OUT
      handler */


….'
  }
….'
  return LPC_OK;
}
```


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3.14 USBROM.2

Introduction:

The USB ROM drivers configure and manage data structures used by the USB controller's DMA engine to move data between the controller's internal fifos and system memory. The configuration of these data structures are based on many parameters including the type of transfer, control, bulk, interrupt, or isochronous, that is to be performed. These data structures reside in system RAM on a 2 kB boundary and are pointed to by the ENDPOINTLISTADDR register.

Problem:

The USB ROM drivers incorrectly configures the Endpoint Capabilities/Characteristics field of the device Queue Head (dQH) structure for isochronous endpoints. Specifically, the MULT member is set to 0 and the ZLT member is set to 1. Also if the maximum size of isochronous packets are 1024 bytes the Max_packet_length member will be set to 0. For any other packet size this member is set correctly.

Work-around:

To use isochronous transfers with the USB ROM drivers the Endpoint Capabilities/Characteristics field must be correctly configured for that endpoint's device Queue Head structure. The USB ROM driver always sets this field (incorrectly) when the host sends a Set Interface control packet and then it calls the USB_Interface_Event callback routine, so the field must be set with the proper value in this callback routine.

This is the device Queue Head structure:

```
typedef volatile struct
{
  volatile uint32_t cap;
  volatile uint32_t curr_dTD;
  volatile uint32_t next_dTD;
  volatile uint32_t total_bytes;
  volatile uint32_t buffer0;
  volatile uint32_t buffer1;
  volatile uint32_t buffer2;
  volatile uint32_t buffer3;
  volatile uint32_t buffer4;
  volatile uint32_t reserved;
  volatile uint32_t setup[2];
  volatile uint32_t gap[4];
}  DQH_T;
```

This is an Interface Event callback routine:

```
ErrorCode_t USB_Interface_Event (USBD_HANDLE_T hUsb)
{
     USB_CORE_CTRL_T* pCtrl = (USB_CORE_CTRL_T*)hUsb;
     uint16_t wIndex = pCtrl->SetupPacket.wIndex.W; // Interface number
     uint16_t wValue = pCtrl->SetupPacket.wValue.W; // Alternate setting number

     if (wIndex == isochronous_interface_number && wValue == 1)
     {
```


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```
            DQH_T* ep_QH = *(DQH_T**)0x40006158; // ENDPOINTLISTADDR register
            int QH_idx = ((endpoint_address & 0x0F) << 1) + 1;

            ep_QH[QH_idx].cap = ((packets_executed_per_transaction_descriptor << 30) |
      (maximum_packet_size << 16));
      }

  return LPC_OK;
}
```

The value of isochronous_interface_number should correspond to the interface number in the USB descriptor that holds the isochronous endpoint you wish to use.

The value of maximum_packet_size should correspond to the wMaxPacketSize member of the isochronous endpoint descriptor

The value of endpoint_address should correspond to the bEndpointAddress member of the isochronous endpoint descriptor

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3.15 SD/MMC.1

Introduction:

The LPC43xx parts have the SD/MMC interface. After power up, the SD memory card is in the default speed mode, and by using the Switch Function command (CMD6), Version 1.10 and higher, the SD memory cards can be placed in high-speed mode. In response to the CMD6 command, the SD card returns a 512-bit block of data containing the available features and actual settings. The SDIO interface is setup for 4-bit data and therefore, the 512 bits are returned on the four data lines in 128 clocks followed by 16 clocks of CRC data.

Problem:

The CMD6 returned status block always gets a data CRC error although the status data is correct. The data CRC error prevents the switching of the SD memory card from the default mode to high-speed mode.

Work-around:

Capture the 64 bits of CRC data that follow the 512 bits of data allowing the CRC data to be calculated in software. The DMA buffer length and SD/MMC BYTCNT must be set to 72 (versus 64). The CRC data consists of four interleaved 16-bit words, one for each of the four serialized SD data bits. If all four of the calculated CRCs match the captured CRCs, the software can clear the data CRC error flag bit.

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3.16 RESET.1

Introduction:

The LPC43xx parts contain a Reset Generation Unit (RGU) that generates various resets; Core Reset (CORE_RST), Peripheral Reset (PERIPH_RST), Master Reset (MASTER_RST), and M4 Reset (M4_RST).

Problem:

On the LPC43xx, MASTER_RST and M4_RST are not functional.

Work-around:

There is no work-around. To reset the entire chip use the CORE_RST instead of using MASTER_RST or M4_RST.

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3.17 RESET.2

Introduction:

The LPC43xx parts contain a Reset Generation Unit (RGU) that generates various resets; Core Reset (CORE_RST), Peripheral Reset (PERIPH_RST), Master Reset (MASTER_RST), and M4 Reset (M4_RST).

Problem:

On the LPC43xx, PERIPH_RST is not functional. CMSIS call NVIC_SystemReset() uses PERIPH_RST internally and is also non-functional.

Work-around:

There is no work-around. To reset the entire chip, use the CORE_RST instead of using CMSIS call NVIC_SystemReset() or PERIPH_RST.

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3.18 RESET.3

Introduction:

The LPC43xx devices are initialized after a reset. If a reset occurs via nRESET pin when the part is in deep-sleep or power-down mode, the initialization state of the device may be erroneous and some functionality of the device may be lost.

Problem:

When the part is in deep-sleep or power-down mode and if an external reset occurs via nRESET pin being activated, as the part comes out of reset, the reset state of some functional blocks may be incorrect. This may result in loss of functionality of the device. The actual functionality lost may vary from part to part depending on the erroneous reset state of the functional blocks. The possible affected blocks are: Ethernet, LCD controller, CAN0, CAN1, USB0, USB1, SGPIO, AES, Cortex-M0 coprocessor and Cortex-M0 subsystem (if present), 12-bit ADC, SRAM size at 0x2000 0000 may change to 16 kB, SRAM size at 0x2000 8000 may change to 0 kB, and SRAM size at 0x2000 C000 may change to 0 kB.

Work-around:

There are two possible work-arounds:

1. In the application software, before initializing peripherals, the code should assert a soft reset using the following steps:
   a. Read the value in power-down modes register (PD0_SLEEP0_MODE).
   b. If the value in the PD0_SLEEP0_MODE0 register represents deep-sleep mode or power-down mode, then the user should check if a reset event occurred on the nRESET pin (bit ‘19’ in the Event Status register).
   c. If the reset event occurred, the software should set the PD0_SLEEP0_MODE register to deep power-down mode and assert a soft reset using the CORE_RST (bit ‘0’ in the RESET_CTRL0 register).

```
/* Check if wake up event happens in deep Sleep or power Down mode */
    if((LPC_PMC->PD0_SLEEP0_MODE == PMC_PWR_DEEP_SLEEP_MODE)
|| (LPC_PMC->PD0_SLEEP0_MODE == PMC_PWR_POWER_DOWN_MODE))
    {
        /* Check if the wake up event is due to nRESET pin in Event router */
        if(LPC_EVRT->STATUS & (1<<19))
        {
            /* Set power state in PMC */
            LPC_PMC->PD0_SLEEP0_MODE = PMC_PWR_DEEP_POWER_DOWN_MODE;
            /* Set CORE_RST in RGU */
            LPC_RGU->RESET_CTRL0 = (1<<0);
        }
    }
```

2. To initialize the device correctly, assert a second external reset signal to the nRESET pin after 20 μs from the first reset.

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3.19 OTP.1

Introduction:

The LPC43xx parts contain OTP memory with four banks of 128 bits each. The first bank (OTP bank 0) is reserved. The other three OTP banks are programmable. The OTP banks can be programmed (0 → 1) via APIs provided in the ROM.

Problem:

On all packages, repeated power cycling of the device may cause erroneous programming of the OTP banks. During ramp-up, the VDDREG supply voltage does not have enough time to settle and initialize the OTP controller before valid programming voltage is reached on the VPP pin. This may cause accidental programming of the OTP banks. Accidental programming of the OTP banks does not occur during Power-down of the supply voltage.

Work-around:

There are two possible work-arounds to avoid accidental programming of the OTP banks:

1. Ensure supply ramp-up time of 2 ms or greater:
   a. For all packages, except BGA256, if the VDDREG, VDDIO, and VDDA pins are tied together, the supply voltage must have a linear ramp-up time of at least 2 ms. If the VDDREG, VDDA, and VDDIO pins are not tied together, follow the work-around in List item 2 “Delay VDDIO and RESETN pin:”
   b. On the BGA256 package, if OTP programming is required, the voltage on the VPP pin should be delayed by 2 ms after the power supply on the VDDREG, VDDA, and VDDIO pins reaches the operating voltage level. If the VPP pin is tied to VDDREG, VDDA, and VDDIO pins, the supply voltage must have a linear ramp-up time of at least 2 ms. If OTP programming is not required on the BGA256 package, the VPP pin should be left as No-Connect (NC) because the VPP and VDDIO pins are separate.
2. Delay VDDIO and RESETN pin:

   The power supplied to the VDDIO pin should be delayed by 2 ms after the power supply on the VDDREG and VDDA pins stabilizes at the operating voltage level. If booting from external sources (USARTx, SPIFI, EMC, USBx, SPI), the signal to the RESETN pin must also be delayed by 2 ms after the power supply on the VDDIO pin stabilizes at the operating voltage level. The following circuit diagram is an example that shows the P-channel MOSFET with the gate delayed and the R-C delay circuit connected to the RESETN pin.

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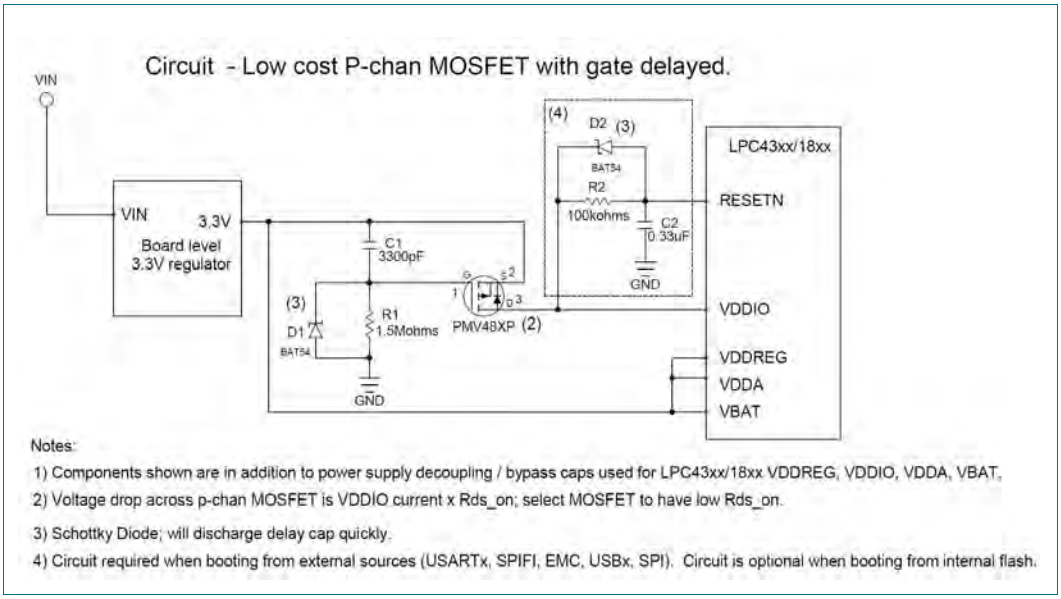
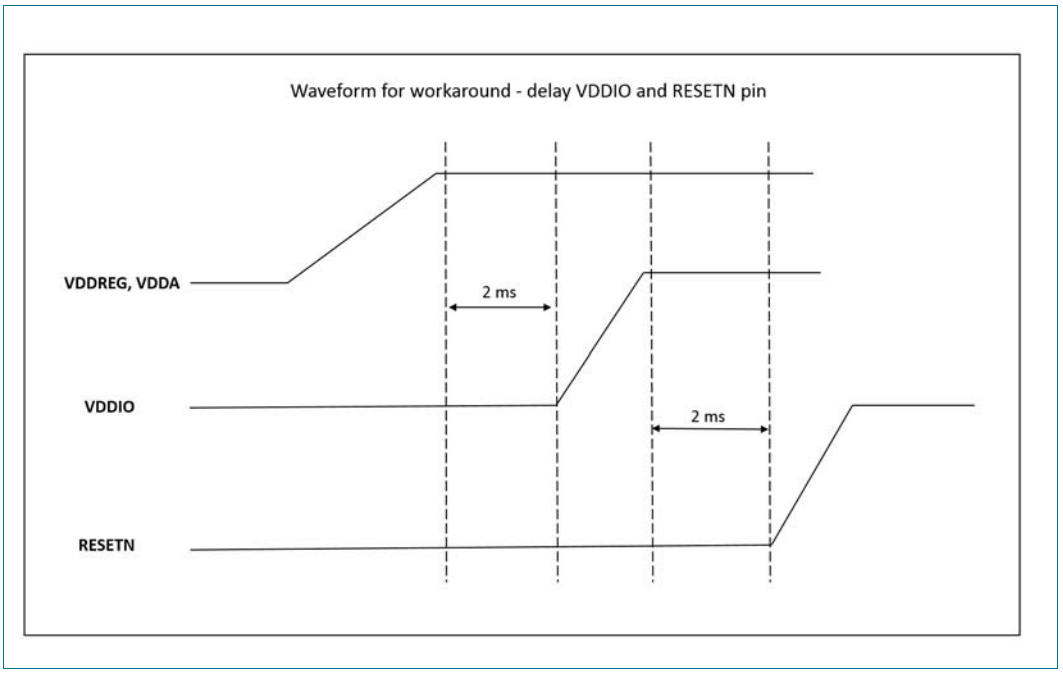


For this problem, there is no restriction on the VBAT supply.

The following diagram shows the waveform for the work-around in List item 2 “Delay VDDIO and RESETN pin:”



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4. AC/DC deviations detail

4.1 IBAT.1

Introduction:

The LPC43xx flash-based devices contain a Real-Time Clock which measures the passage of time. The RTC has an ultra-low power design to support battery powered systems with a dedicated battery supply pin.

Problem:

On the LPC43xx flash-based devices, high current consumption of about 70 μA or higher may occur on the VBAT power supply pin due to current drain from the RTC_ALARM and SAMPLE pins.

On the LPC43xx flash-based devices, at temperatures lower than 0 °C, high current consumption up to 25 μA may occur on the VBAT power supply pin while VDD is present if VDD < VBAT. This is seen during Deep Sleep, Power Down, and Deep Power Down modes.

Work-around:

VBAT current consumption due to RTC_ALARM and SAMPLE pins can be lowered significantly by configuring the RTC_ALARM pin and SAMPLE pins as "Inactive" by setting the ALARMCTRL 7:6 field in CREG0 to 0x3 and the SAMPLECTRL 13:12 field in CREG0 to 0x3. These bits persist through power cycles and reset, as long as VBAT is present.

To work-around the current consumption at temperatures less than 0 °C, keep the VBAT voltage less than VDD. For example, use a 3.0 V VBAT voltage with a 3.3 V VDD supply. This also avoids current consumption during active mode which can occur when VBAT > VDD (see the *LPC435X_3X_2X_1X data sheet* for details).

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6. Contents

1 Product identification 3
2 Errata overview 3
3 Functional problems detail 5
3.1 C_CAN.1 5
3.2 EEPROM.2 6
3.3 EMC.1 7
3.4 EMC.2 8
3.5 I2C.1 9
3.6 ISP.1 10
3.7 MCPWM.1 11
3.8 PMC.1 12
3.9 PMC.2 13
3.10 SRAM.1 14
3.11 USB.1 15
3.12 USB.2 16
3.13 USBROM.1 17
3.14 USBROM.2 19
3.15 SD/MMC.1 21
3.16 RESET.1 22
3.17 RESET.2 23
3.18 RESET.3 24
3.19 OTP.1 25
4 AC/DC deviations detail 27
4.1 IBAT.1 27
5 Legal information 28
5.1 Definitions 28
5.2 Disclaimers 28
5.3 Trademarks 28
6 Contents 29

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